

Claims

1. A heterostructure containing the semiconductor alloys $\text{Ga}_x\text{In}_{1-x}\text{As}$ and $\text{InAs}_y\text{P}_{1-y}$ for minimizing dislocations resulting from lattice mismatch of an active, heteroepitaxial layer, the
5 heterostructure comprising:
 - a semi-insulating substrate;
 - a compositionally step-graded region terminated by a buffer layer;
 - a intermediate region;
 - an active layer; and
 - 10 a capping layer.
2. The heterostructure of claim 1 wherein the substrate is constructed from InP.
3. The heterostructure of claim 1 wherein the step-graded region is constructed from $\text{InAs}_y\text{P}_{1-y}$.
4. The heterostructure of claim 3 wherein the composition within the $\text{InAs}_y\text{P}_{1-y}$ step-graded region is varied incrementally thereby accommodating the mismatch of the active layer.
- 15 5. The heterostructure of claim 1 wherein the buffer layer is constructed from $\text{InAs}_y\text{P}_{1-y}$.
6. The heterostructure of claim 5 wherein the strained $\text{InAs}_y\text{P}_{1-y}$ buffer layer is grown to a thickness of approximately one (1) μm .
7. The heterostructure of claim 1 wherein the active layer is constructed from $\text{Ga}_x\text{In}_{1-x}\text{As}$.
8. The heterostructure of claim 7 wherein the $\text{Ga}_x\text{In}_{1-x}\text{As}$ active layer is deposited upon the
20 buffer layer.
9. The heterostructure of claim 1 wherein the capping layer is constructed from $\text{InAs}_y\text{P}_{1-y}$.
10. The heterostructure of claim 9 wherein the $\text{InAs}_y\text{P}_{1-y}$ capping layer is grown for electrical passivation.
11. The heterostructure of claim 1 wherein the active layer is constructed from epitaxial
25 $\text{Ga}_x\text{In}_{1-x}\text{As}$ with $x < 0.47$, and the step-graded region and buffer layer are constructed from $\text{InAs}_y\text{P}_{1-y}$.
12. The heterostructure of claim 1 wherein each of the layers is deposited with a vapor-phase epitaxy technique.

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13. A method for eliminating strain and dislocations resulting from lattice mismatch of a heteroepitaxial layer, the method comprising:
- providing a semi-insulating substrate;
 - depositing a compositionally step-graded region on the semi-insulating substrate;
 - 5 terminating the step-graded region with a buffer layer;
 - depositing an intermediate region on the buffer layer;
 - depositing an active layer on the buffer layer; and
 - depositing a capping layer on the active layer.
14. The method of claim 13 further comprising: constructing the substrate from InP.
- 10 15. The method of claim 13 further comprising: constructing the step-graded layer from $\text{InAs}_y\text{P}_{1-y}$.
16. The method of claim 15 further comprising: incrementally varying the composition y of the step-graded layer thereby accommodating the mismatch of the heteroepitaxial layer.
17. The method of claim 13 further comprising: constructing the buffer layer from $\text{InAs}_y\text{P}_{1-y}$.
- 15 18. The method of claim 17 further comprising: growing the strained $\text{InAs}_y\text{P}_{1-y}$ buffer layer to a thickness of approximately one (1) μm .
19. The method of claim 13 further comprising: constructing the active layer from $\text{Ga}_x\text{In}_{1-x}\text{As}$.
20. The method of claim 19 further comprising: depositing the $\text{Ga}_x\text{In}_{1-x}\text{As}$ active layer upon the buffer layer.
- 20 21. The method of claim 13 further comprising: constructing the capping layer from of $\text{InAs}_y\text{P}_{1-y}$.
22. The method of claim 21 further comprising: growing the $\text{InAs}_y\text{P}_{1-y}$ capping layer for electrical passivation.
23. The method of claim 13 further comprising: depositing each layer by vapor-phase epitaxy.